



## P-Channel 30-V (D-S) MOSFET

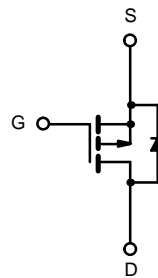
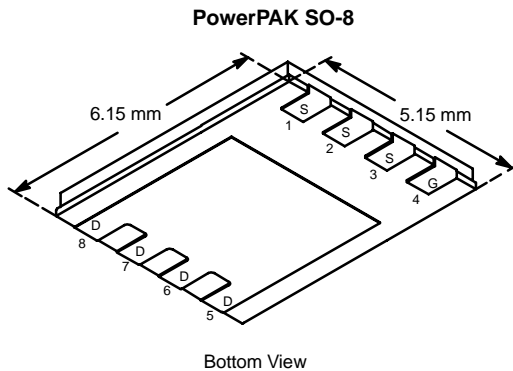
PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
-30	0.0068 @ $V_{GS} = -10$ V	-22

### FEATURES

- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile

### APPLICATIONS

- Battery and Load Switching
  - Notebook Computers
  - Notebook Battery Packs



Ordering Information: Si7459DP-T1 - E3

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	$V_{DS}$	-30		V	
Gate-Source Voltage	$V_{GS}$	$\pm 25$			
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	-22	-13	A
		$T_A = 70^\circ\text{C}$	-17	-10	
Pulsed Drain Current	$I_{DM}$	-60			
continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	-4.5	-1.6		
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	5.4	1.9	W
		$T_A = 70^\circ\text{C}$	3.4	1.2	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 10$ sec	18	23	$^\circ\text{C/W}$
		Steady State	52	65	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	1.0	1.5		

Notes

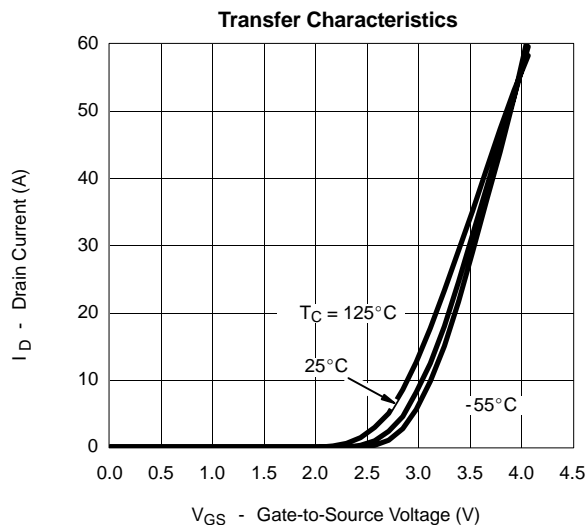
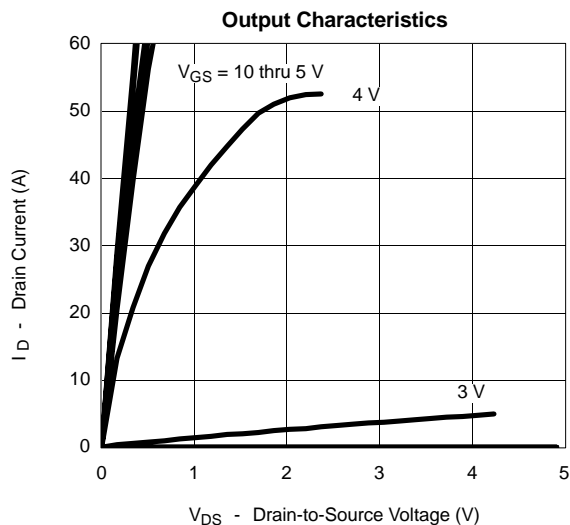
a. Surface Mounted on 1" x 1" FR4 Board.

**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1.0		-3.0	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
		V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±25 V			±200	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V			-1	μA
		V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C			-10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -10 V	-30			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -22 A		0.0056	0.0068	Ω
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -22 A		50		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = -2.9 A, V <sub>GS</sub> = 0 V		-0.71	-1.1	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -22 A		113	170	nC
Gate-Source Charge	Q <sub>gs</sub>			17		
Gate-Drain Charge	Q <sub>gd</sub>			32.5		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -10 V, R <sub>G</sub> = 6 Ω		25	40	ns
Rise Time	t <sub>r</sub>			20	30	
Turn-Off Delay Time	t <sub>d(off)</sub>			180	270	
Fall Time	t <sub>f</sub>			130	200	
Gate Resistance	R <sub>g</sub>			4		Ω
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -2.9 A, di/dt = 100 A/μs		100	150	ns

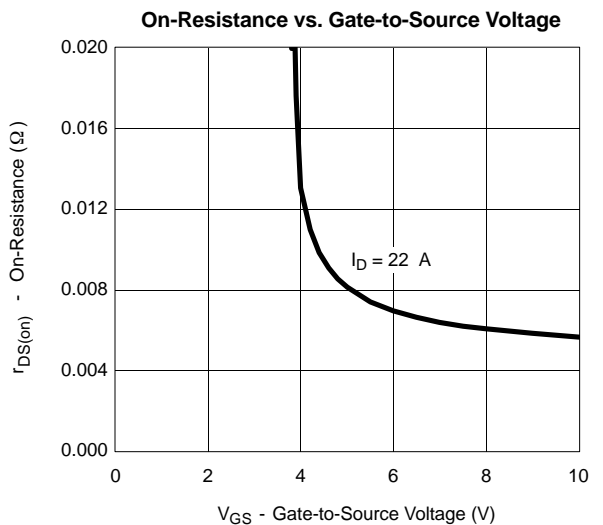
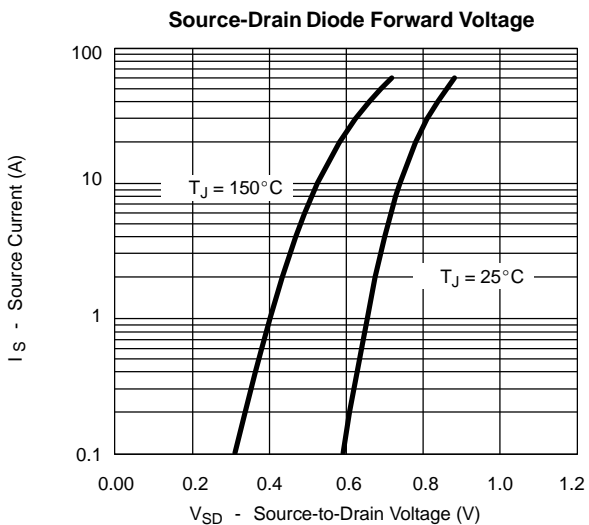
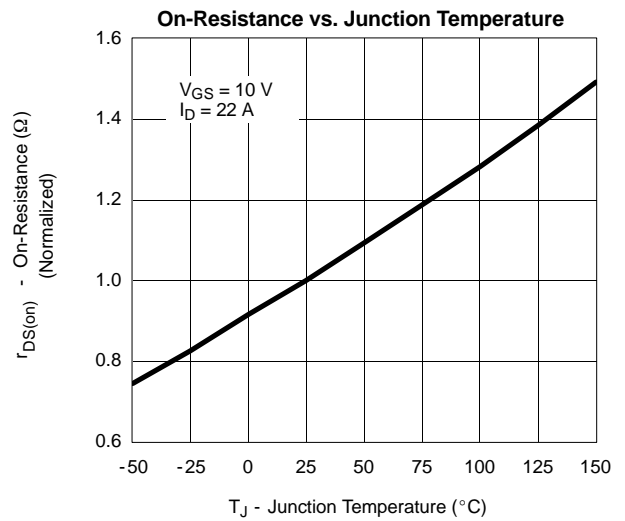
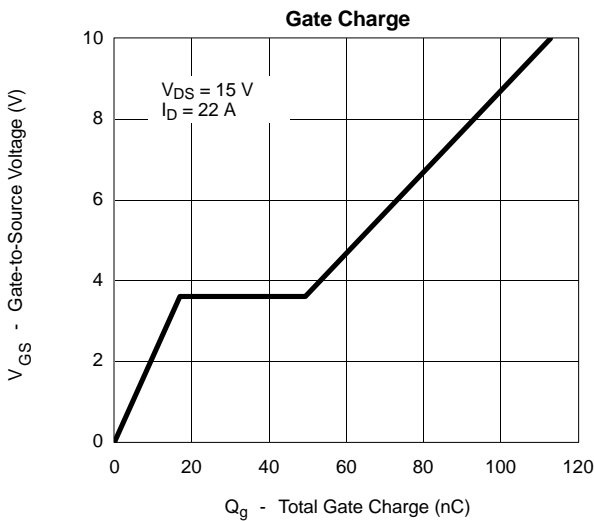
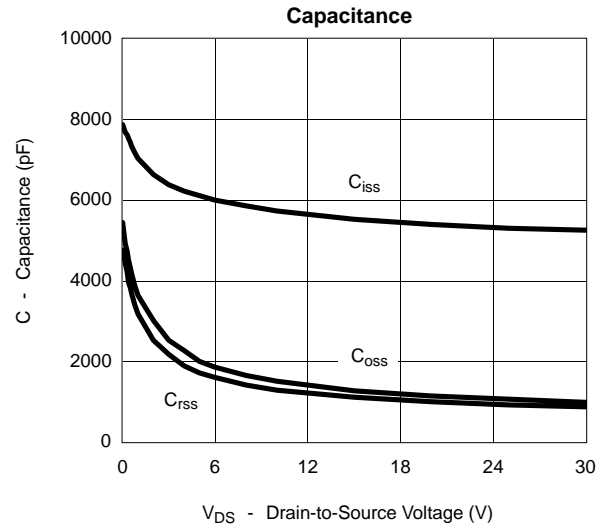
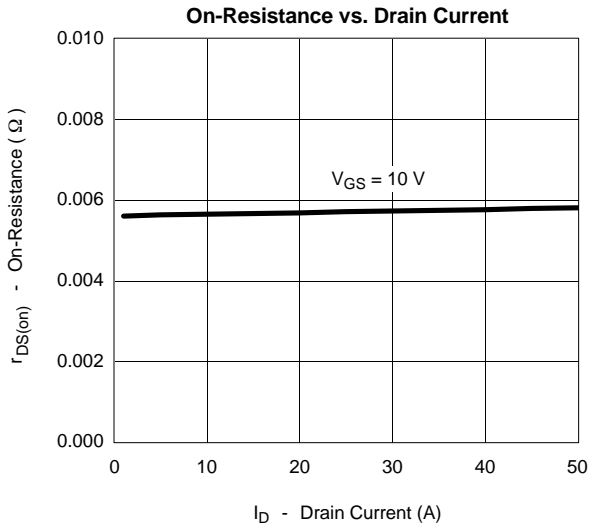
## Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
b. Guaranteed by design, not subject to production testing.

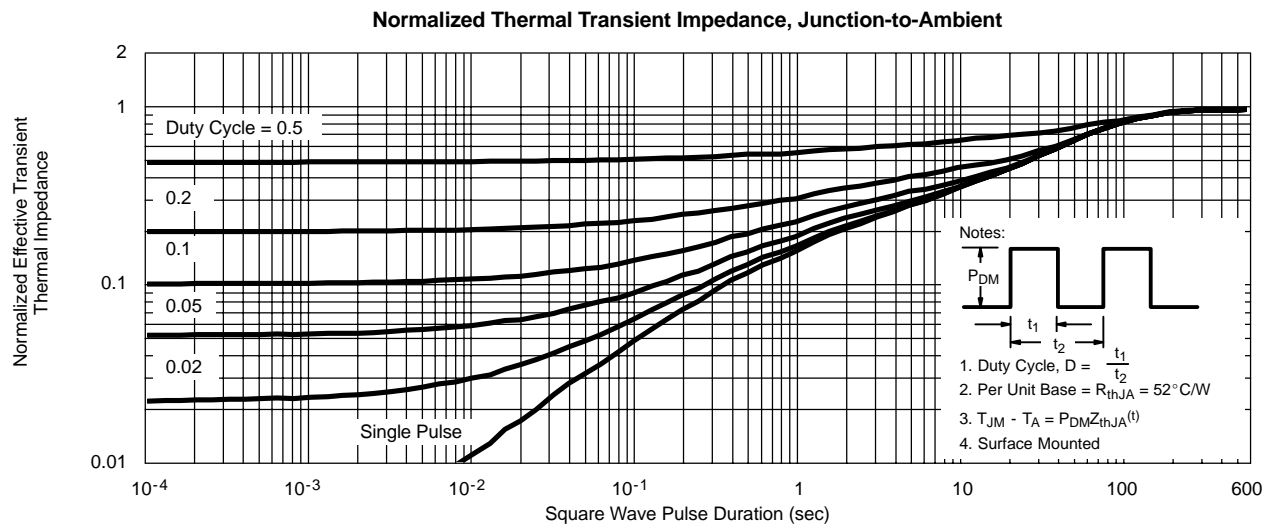
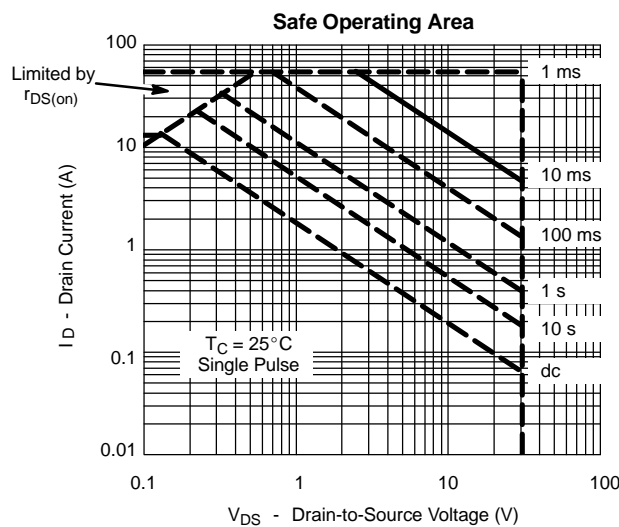
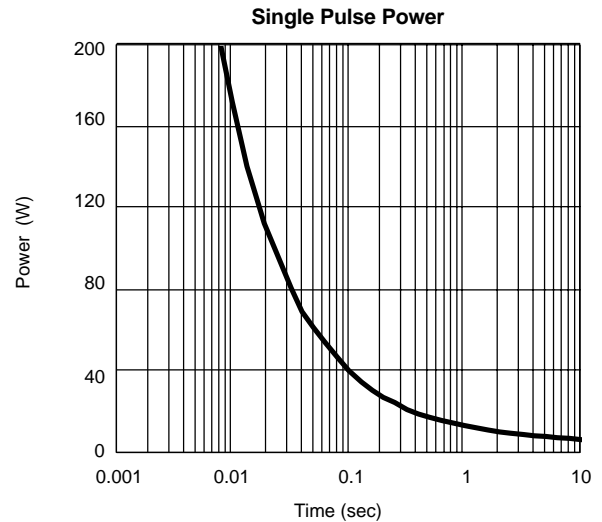
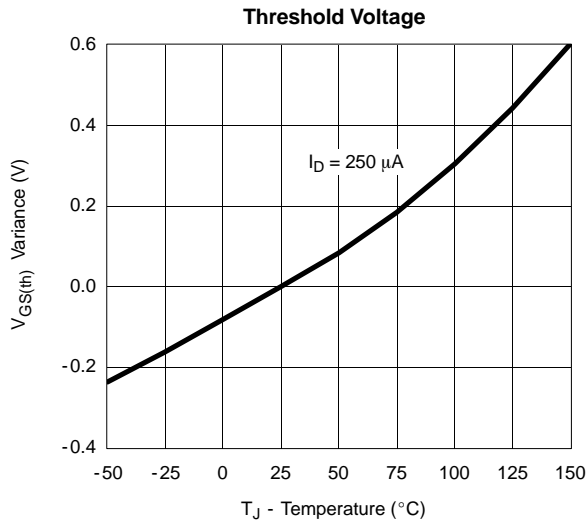
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



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